Amendments to the Specification:

Please replace the paragraph beginning at page 2, line 9, with the following amended paragraph:

~~If~~ It would furthermore be desirable to have a multiprocessor system in which input/output modules and processors are treated as being participants in the general system interconnect and in the cache coherency mechanism. In such a system there would be no need for a special input/output interconnect or bridge, because the input/output modules would communicate data requests and data modifications to the rest of the system via the normal protocol of the cache coherence mechanism. Such a system would furthermore be capable of being configured with an arbitrary ratio of input/output modules and processors.